OIPE IAP47 JUL 19 2006 PATENT & TRADEMARK OFFICE

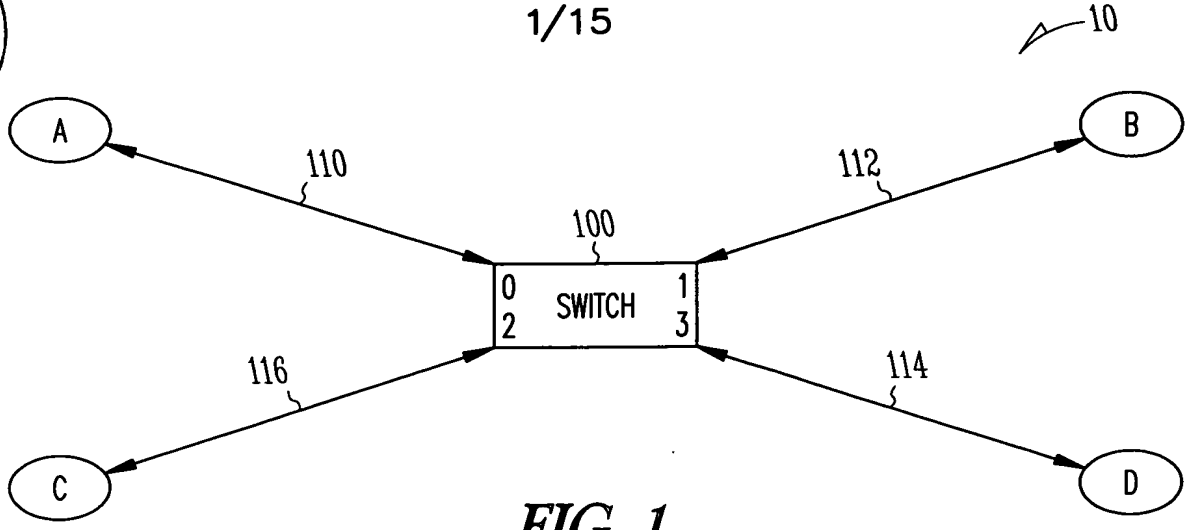


FIG. 1

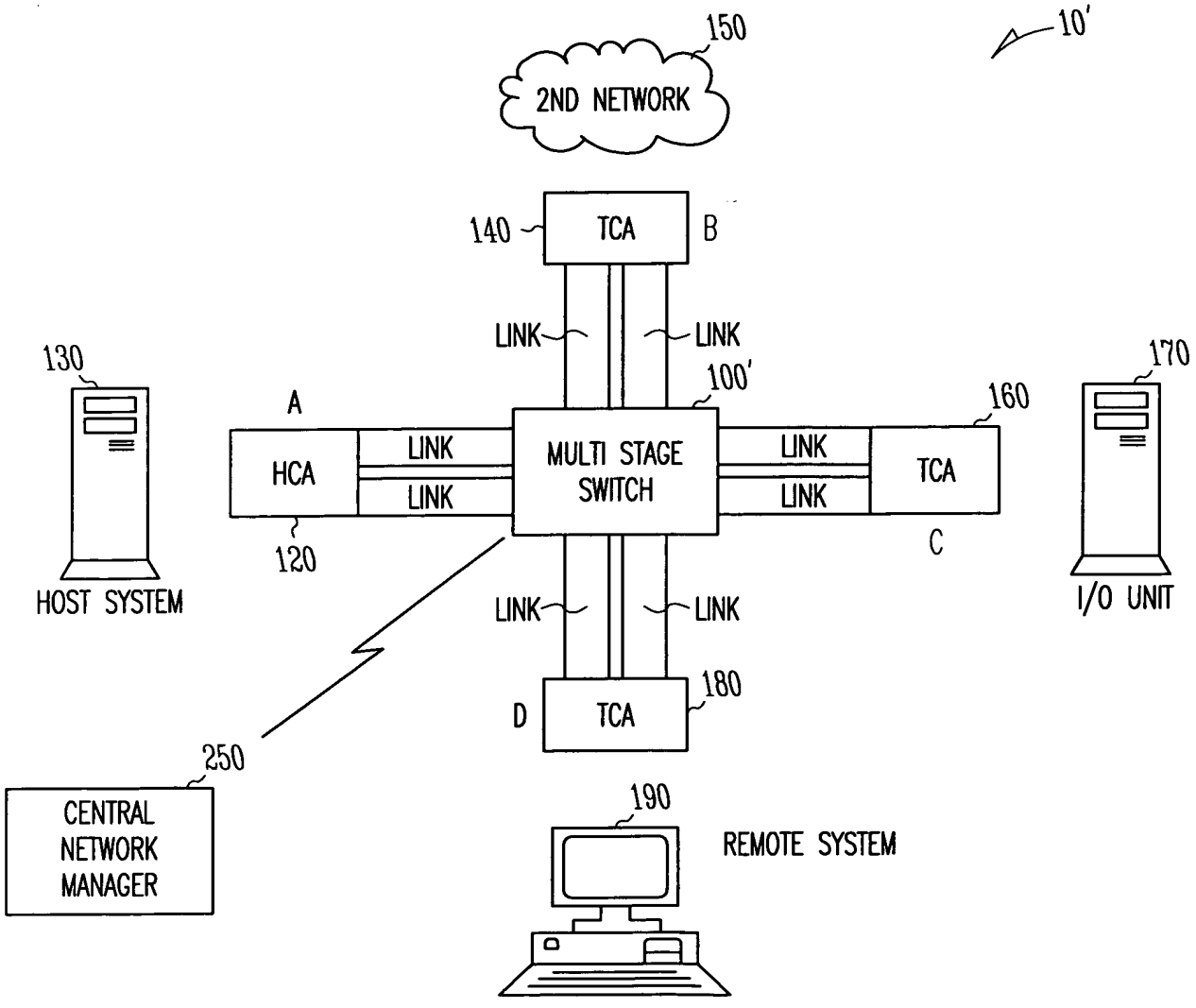
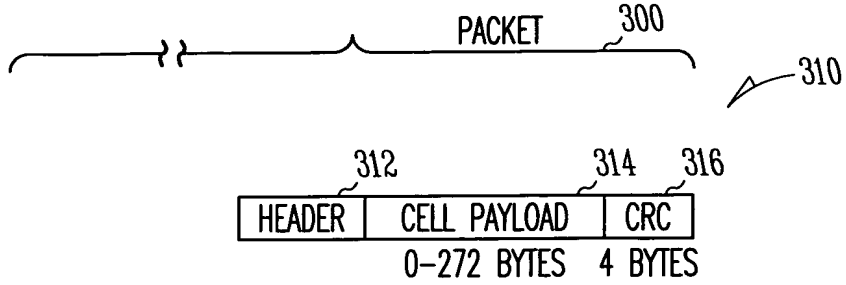


FIG. 2

FIG. 3


PACKET
300
310
312
314
316
HEADER
CELL PAYLOAD
CRC
0-272 BYTES
4 BYTES

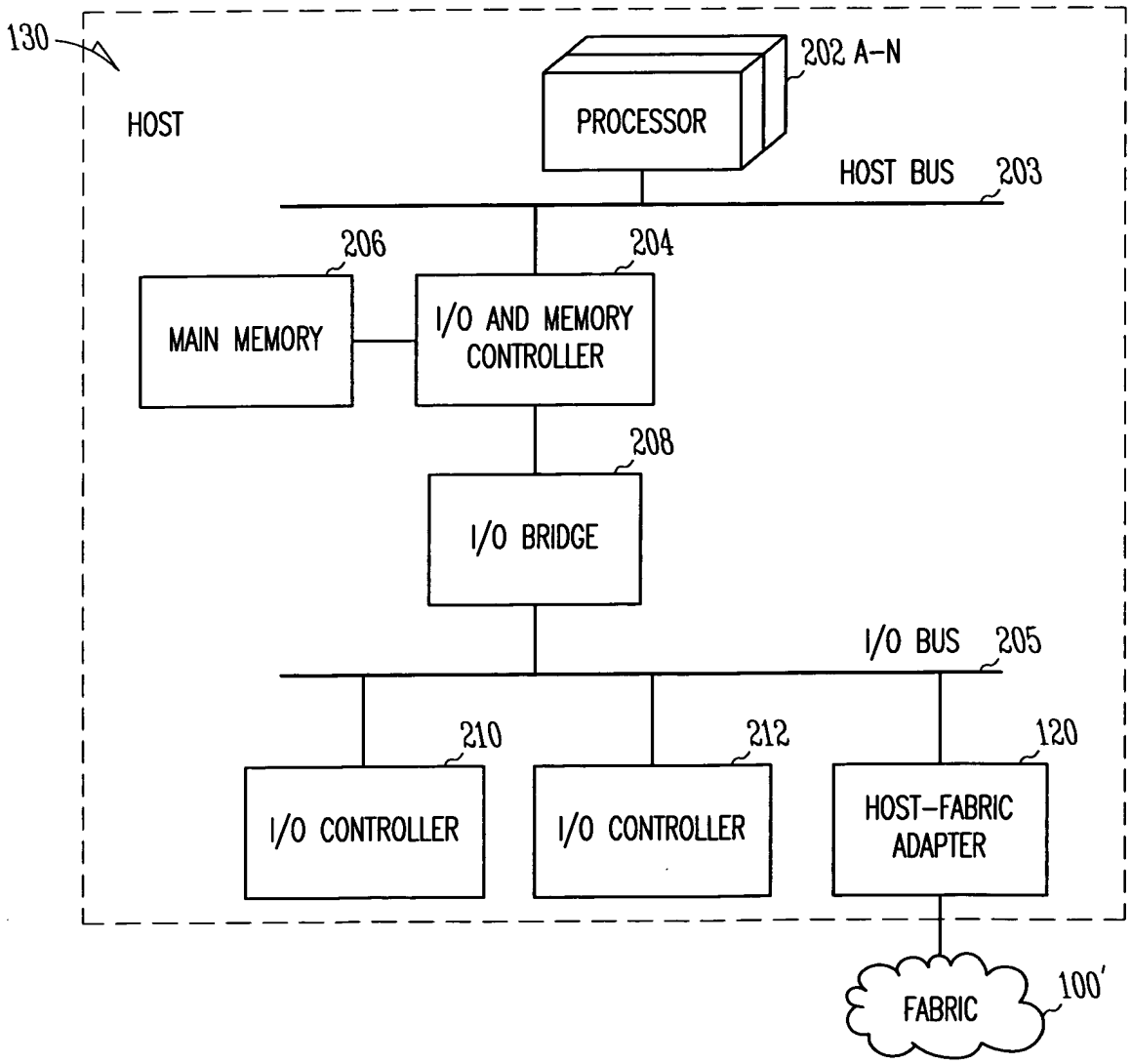

130
HOST
PROCESSOR
202 A-N
HOST BUS
203
206
204
MAIN MEMORY
I/O AND MEMORY CONTROLLER
208
I/O BRIDGE
I/O BUS
205
210
212
120
I/O CONTROLLER
I/O CONTROLLER
HOST-FABRIC ADAPTER
FABRIC
100'

FIG. 4A

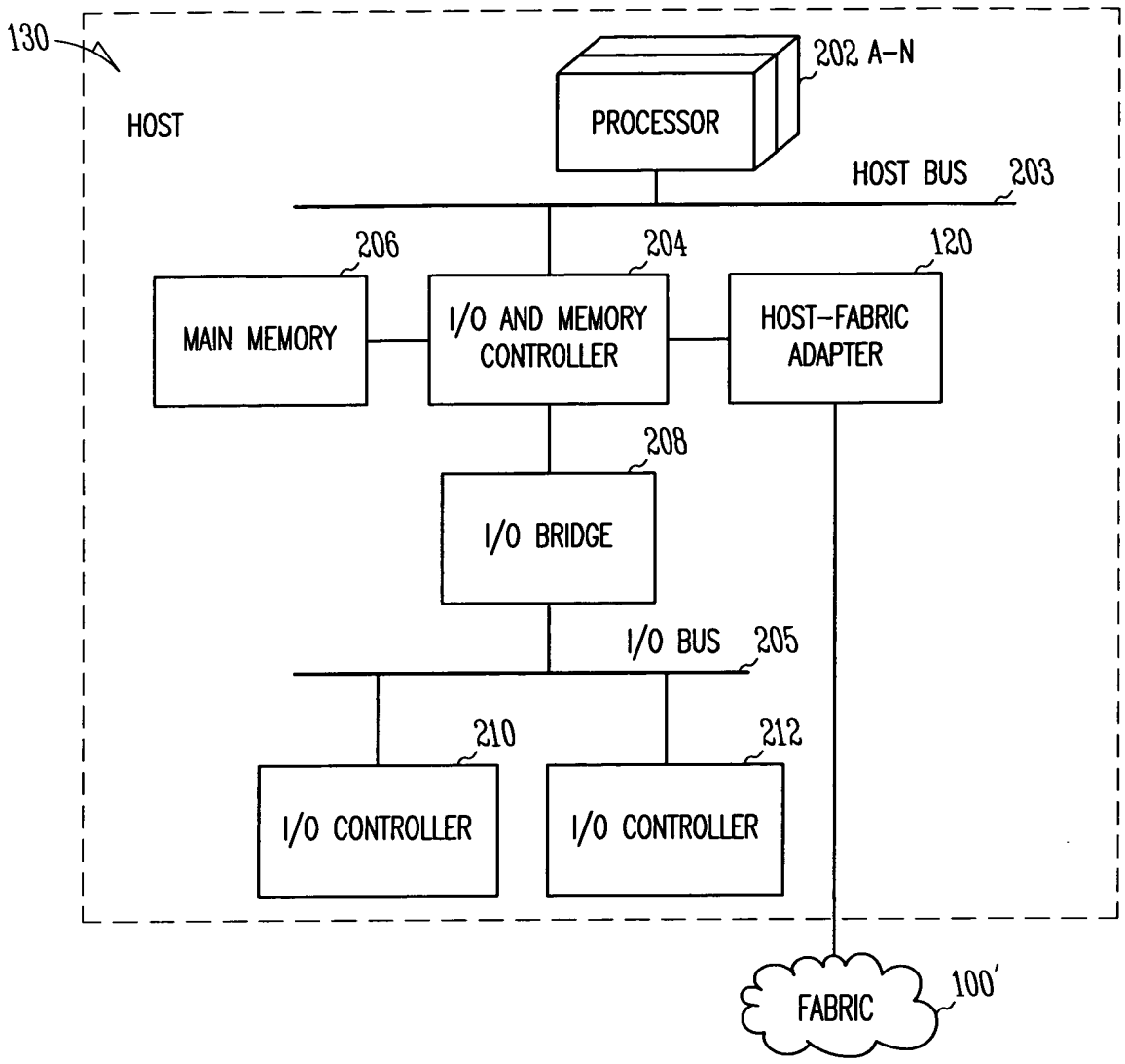

130
HOST
PROCESSOR
202 A-N
HOST BUS
203
206
204
120
MAIN MEMORY
I/O AND MEMORY CONTROLLER
HOST-FABRIC ADAPTER
208
I/O BRIDGE
I/O BUS
205
210
212
I/O CONTROLLER
I/O CONTROLLER
FABRIC
100'

FIG. 4B

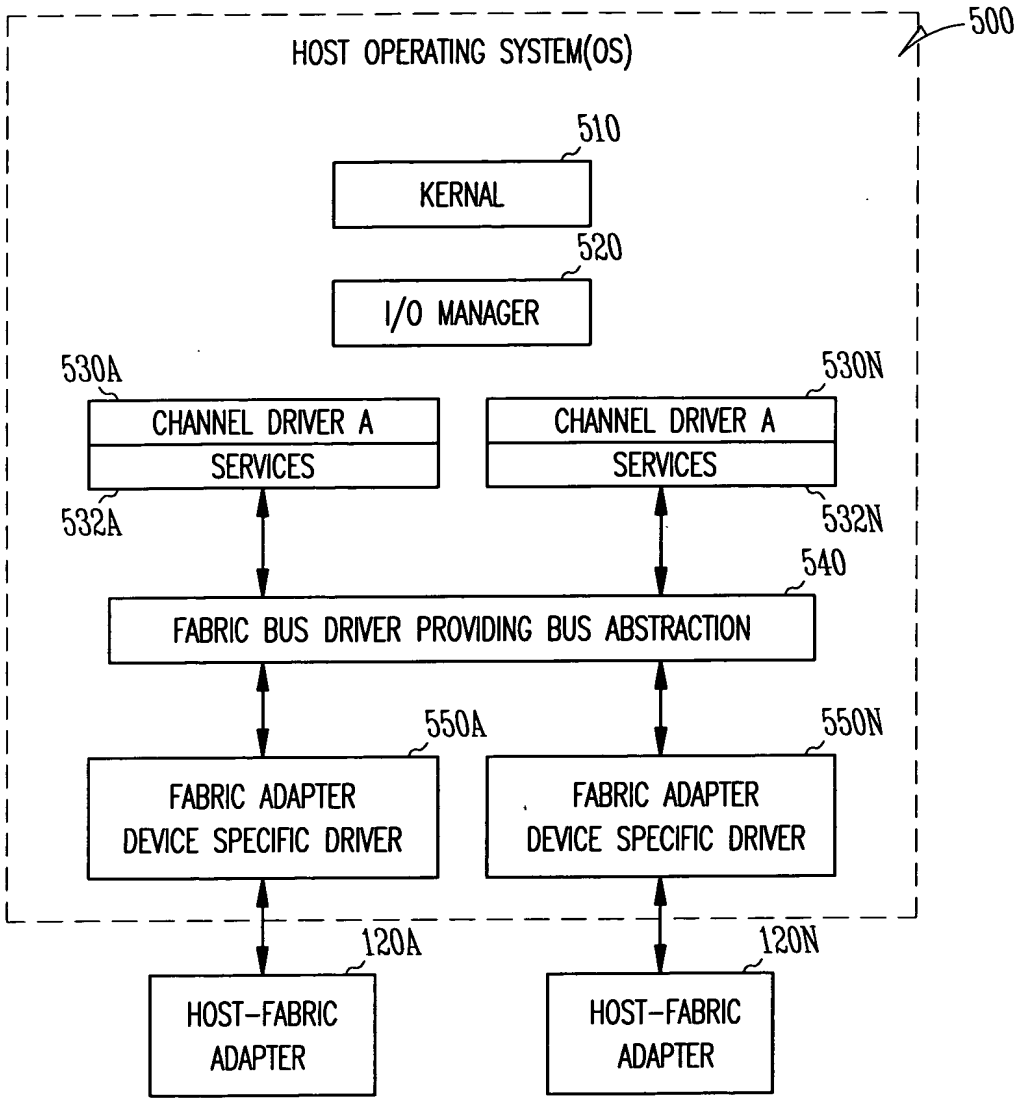

500
HOST OPERATING SYSTEM(OS)
510
KERNAL
520
I/O MANAGER
530A
CHANNEL DRIVER A SERVICES
530N
CHANNEL DRIVER A SERVICES
532A
532N
540
FABRIC BUS DRIVER PROVIDING BUS ABSTRACTION
550A
FABRIC ADAPTER DEVICE SPECIFIC DRIVER
550N
FABRIC ADAPTER DEVICE SPECIFIC DRIVER
120A
HOST-FABRIC ADAPTER
120N
HOST-FABRIC ADAPTER

FIG. 5

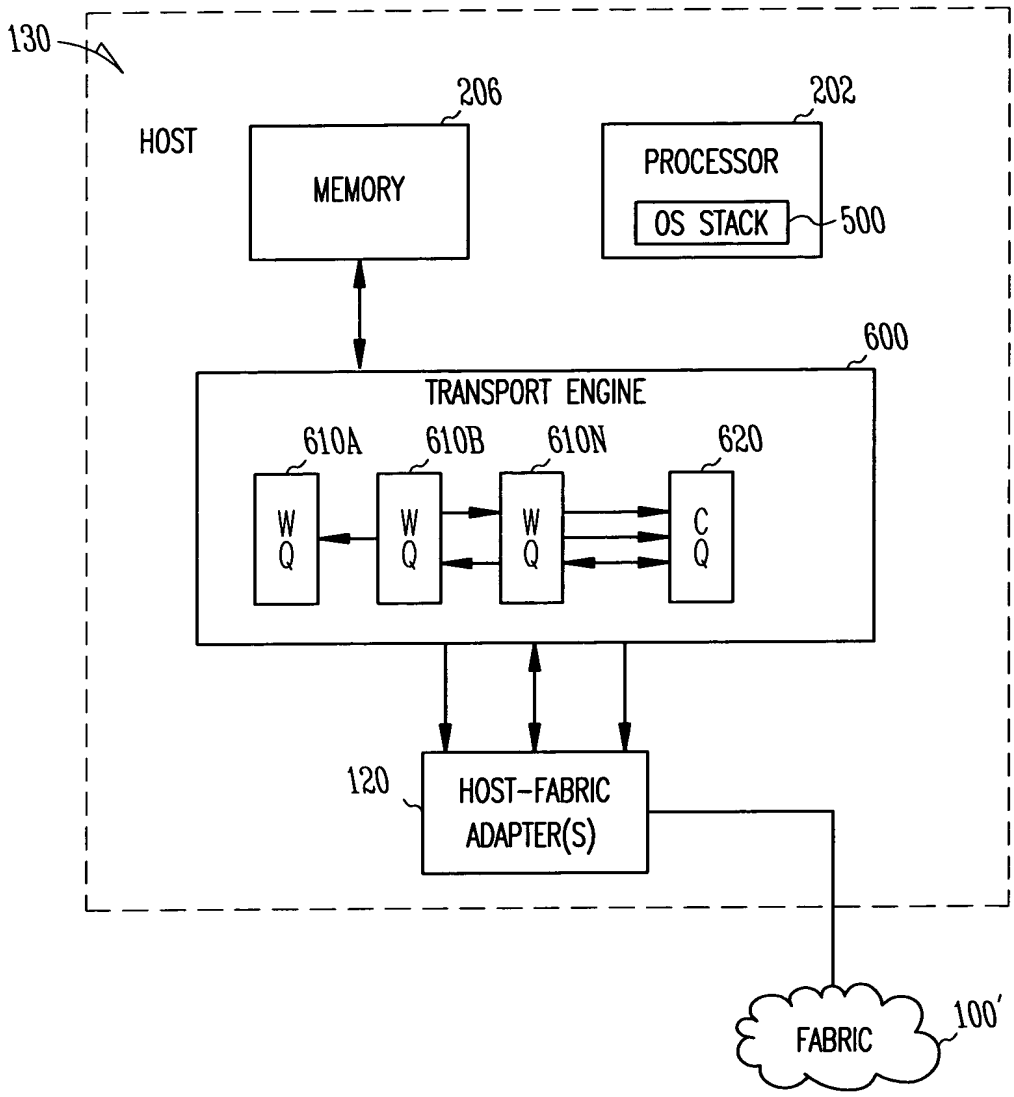

130
HOST
206
MEMORY
202
PROCESSOR
OS STACK
500
600
TRANSPORT ENGINE
610A
610B
610N
620
WQ
WQ
WQ
CQ
120
HOST-FABRIC ADAPTER(S)
FABRIC
100'

FIG. 6

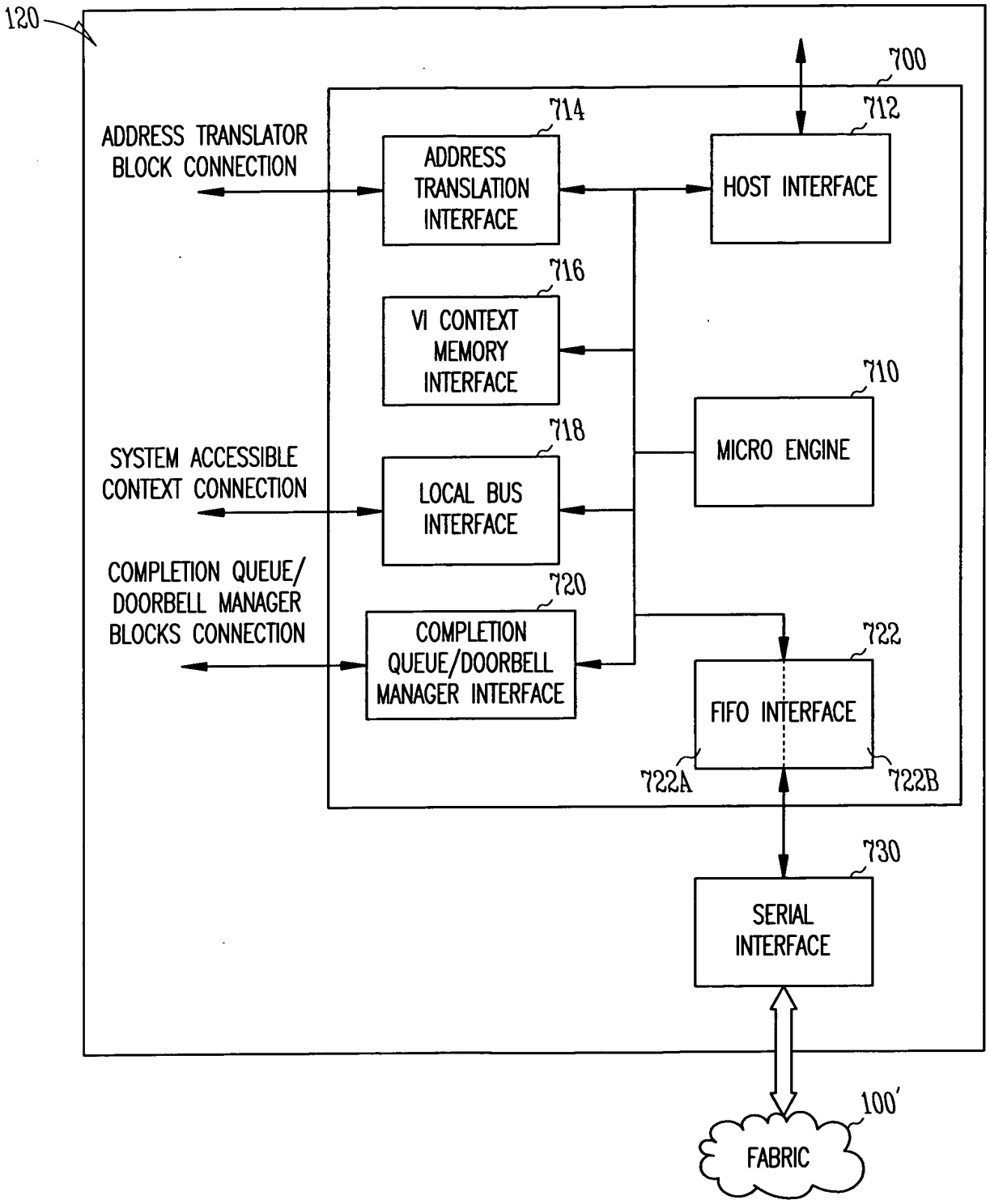

120
700
714
712
ADDRESS TRANSLATOR BLOCK CONNECTION
ADDRESS TRANSLATION INTERFACE
HOST INTERFACE
716
VI CONTEXT MEMORY INTERFACE
710
MICRO ENGINE
718
SYSTEM ACCESSIBLE CONTEXT CONNECTION
LOCAL BUS INTERFACE
COMPLETION QUEUE/ DOORBELL MANAGER BLOCKS CONNECTION
720
COMPLETION QUEUE/DOORBELL MANAGER INTERFACE
722
FIFO INTERFACE
722A
722B
730
SERIAL INTERFACE
100'
FABRIC

FIG. 7

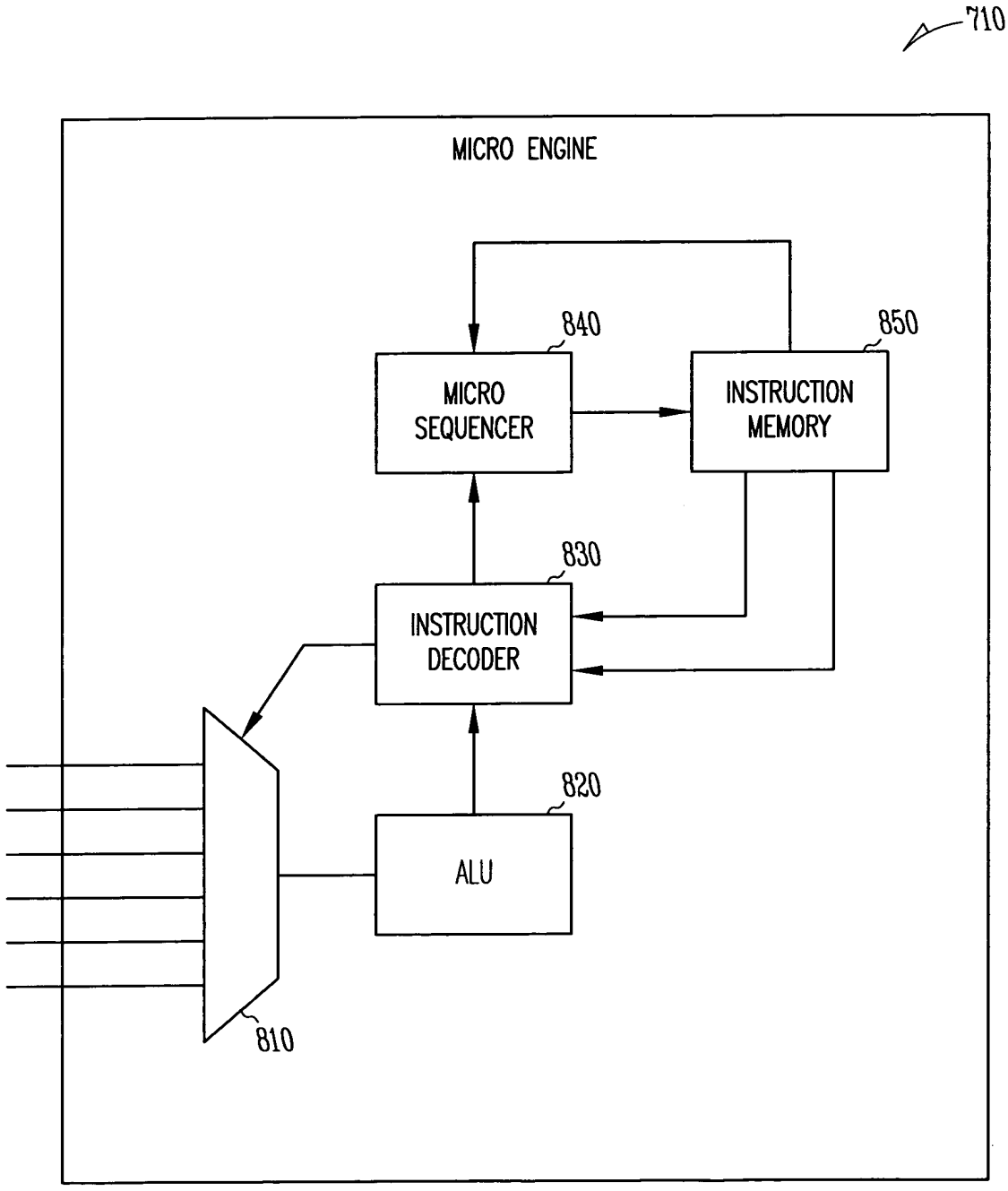

710
MICRO ENGINE
840
MICRO SEQUENCER
850
INSTRUCTION MEMORY
830
INSTRUCTION DECODER
820
ALU
810

FIG. 8

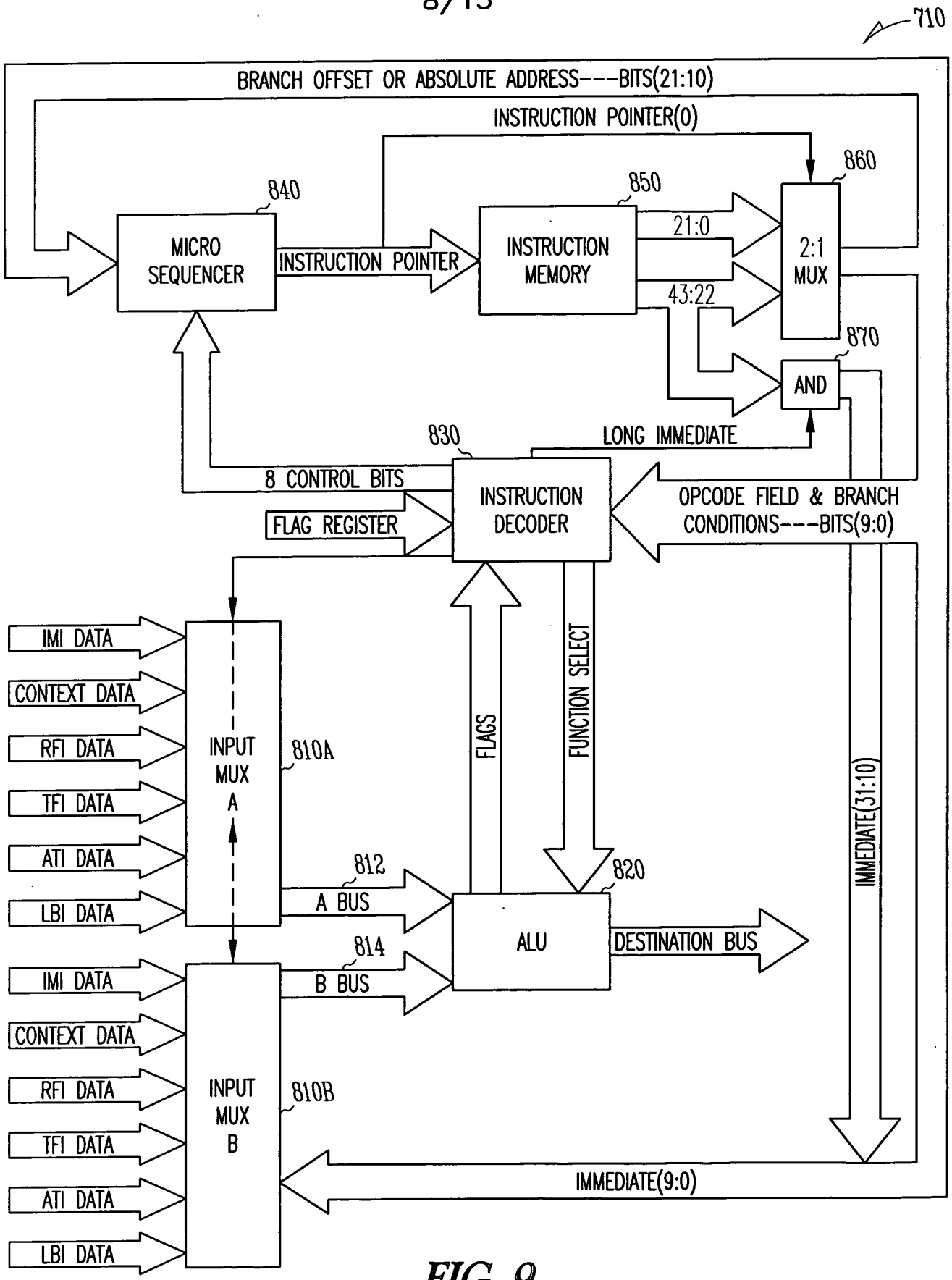

710
BRANCH OFFSET OR ABSOLUTE ADDRESS---BITS(21:10)
INSTRUCTION POINTER(0)
840
MICRO SEQUENCER
INSTRUCTION POINTER
850
INSTRUCTION MEMORY
21:0
43:22
860
2:1 MUX
870
AND
LONG IMMEDIATE
830
8 CONTROL BITS
FLAG REGISTER
INSTRUCTION DECODER
OPCODE FIELD & BRANCH CONDITIONS---BITS(9:0)
IMI DATA
CONTEXT DATA
RFI DATA
TFI DATA
ATI DATA
LBI DATA
INPUT MUX A
810A
FLAGS
FUNCTION SELECT
IMMEDIATE(31:10)
812
A BUS
820
ALU
DESTINATION BUS
814
B BUS
IMI DATA
CONTEXT DATA
RFI DATA
TFI DATA
ATI DATA
LBI DATA
INPUT MUX B
810B
IMMEDIATE(9:0)

FIG. 9

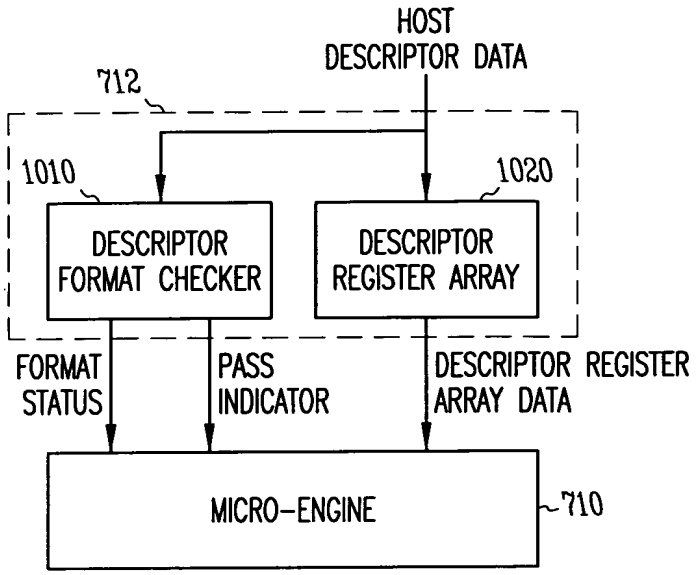


FIG. 10

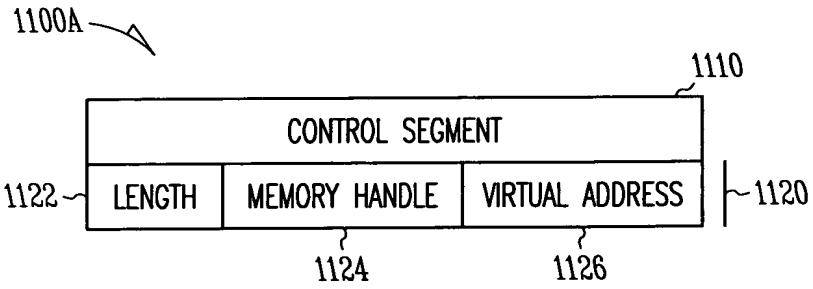


FIG. 11A

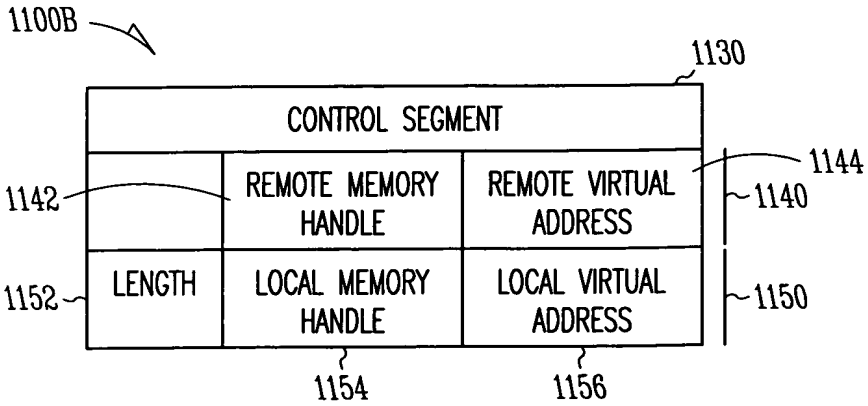


FIG. 11B

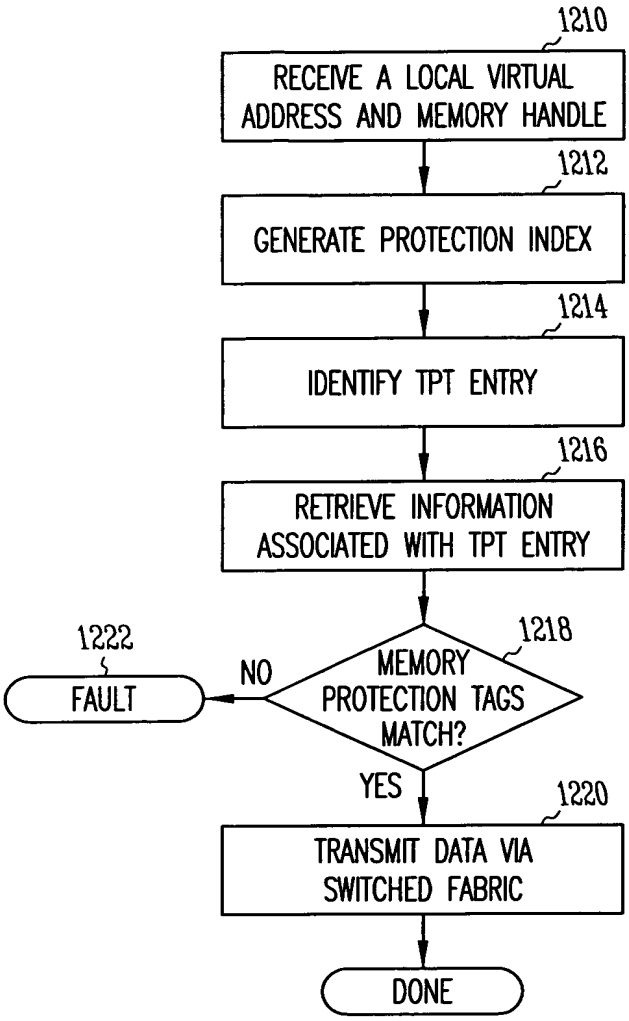

1210
RECEIVE A LOCAL VIRTUAL ADDRESS AND MEMORY HANDLE
1212
GENERATE PROTECTION INDEX
1214
IDENTIFY TPT ENTRY
1216
RETRIEVE INFORMATION ASSOCIATED WITH TPT ENTRY
1218
MEMORY PROTECTION TAGS MATCH?
NO
1222
FAULT
YES
1220
TRANSMIT DATA VIA SWITCHED FABRIC
DONE

FIG. 12

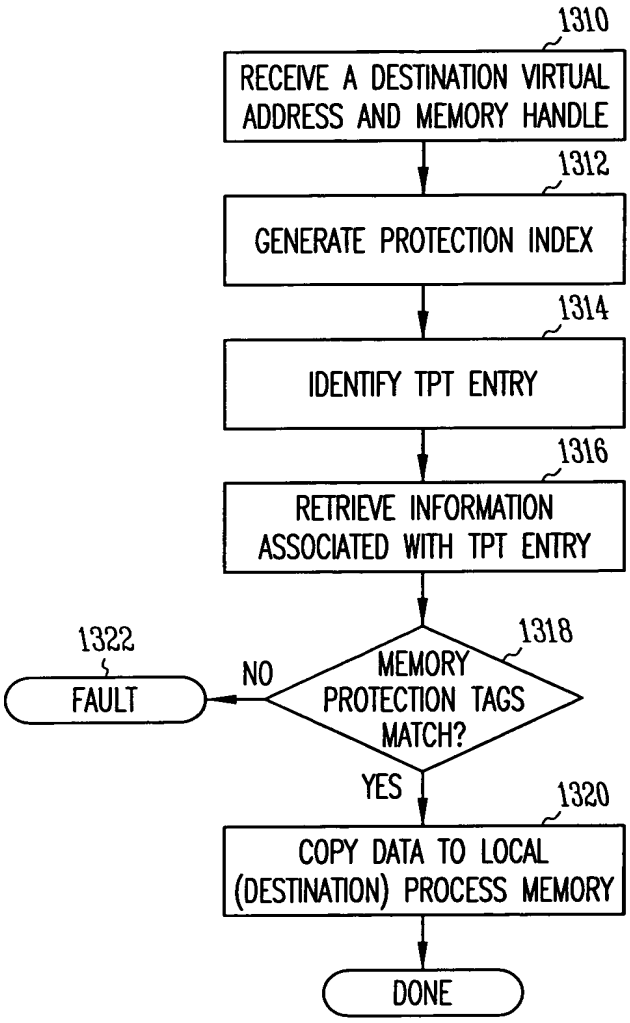

1310
RECEIVE A DESTINATION VIRTUAL ADDRESS AND MEMORY HANDLE
1312
GENERATE PROTECTION INDEX
1314
IDENTIFY TPT ENTRY
1316
RETRIEVE INFORMATION ASSOCIATED WITH TPT ENTRY
1318
MEMORY PROTECTION TAGS MATCH?
NO
1322
FAULT
YES
1320
COPY DATA TO LOCAL (DESTINATION) PROCESS MEMORY
DONE

FIG. 13

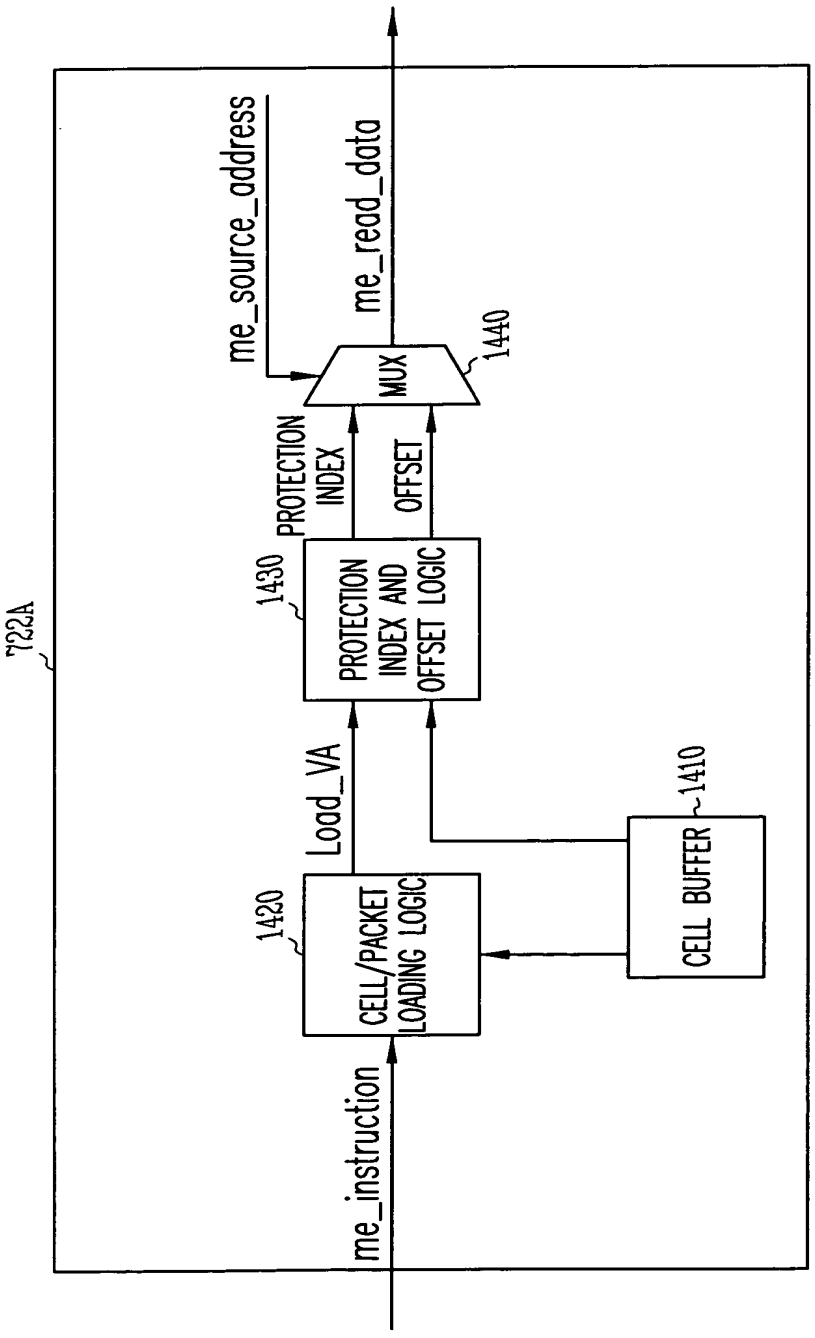

me_source_address
me_read_data
MUX
1440
PROTECTION INDEX
OFFSET
1430
PROTECTION INDEX AND OFFSET LOGIC
722A
Load_VA
1410
CELL BUFFER
1420
CELL/PACKET LOADING LOGIC
me_instruction

FIG. 14

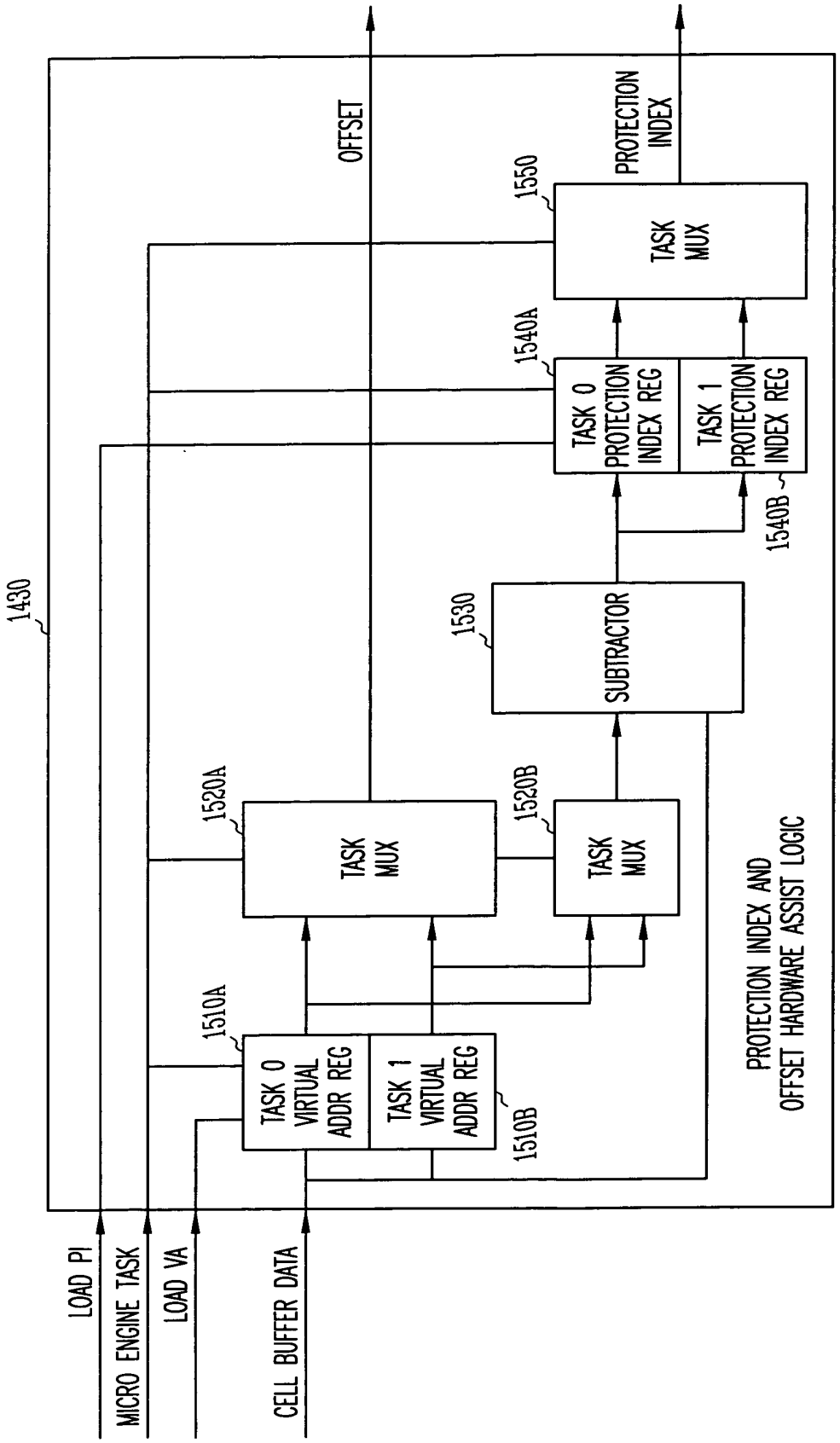

1430
OFFSET
PROTECTION INDEX
1550
TASK MUX
1540A
TASK 0 PROTECTION INDEX REG
TASK 1 PROTECTION INDEX REG
1540B
1530
SUBTRACTOR
1520A
TASK MUX
1520B
TASK MUX
1510A
TASK 0 VIRTUAL ADDR REG
TASK 1 VIRTUAL ADDR REG
1510B
PROTECTION INDEX AND OFFSET HARDWARE ASSIST LOGIC
LOAD PI
MICRO ENGINE TASK
LOAD VA
CELL BUFFER DATA

FIG. 15

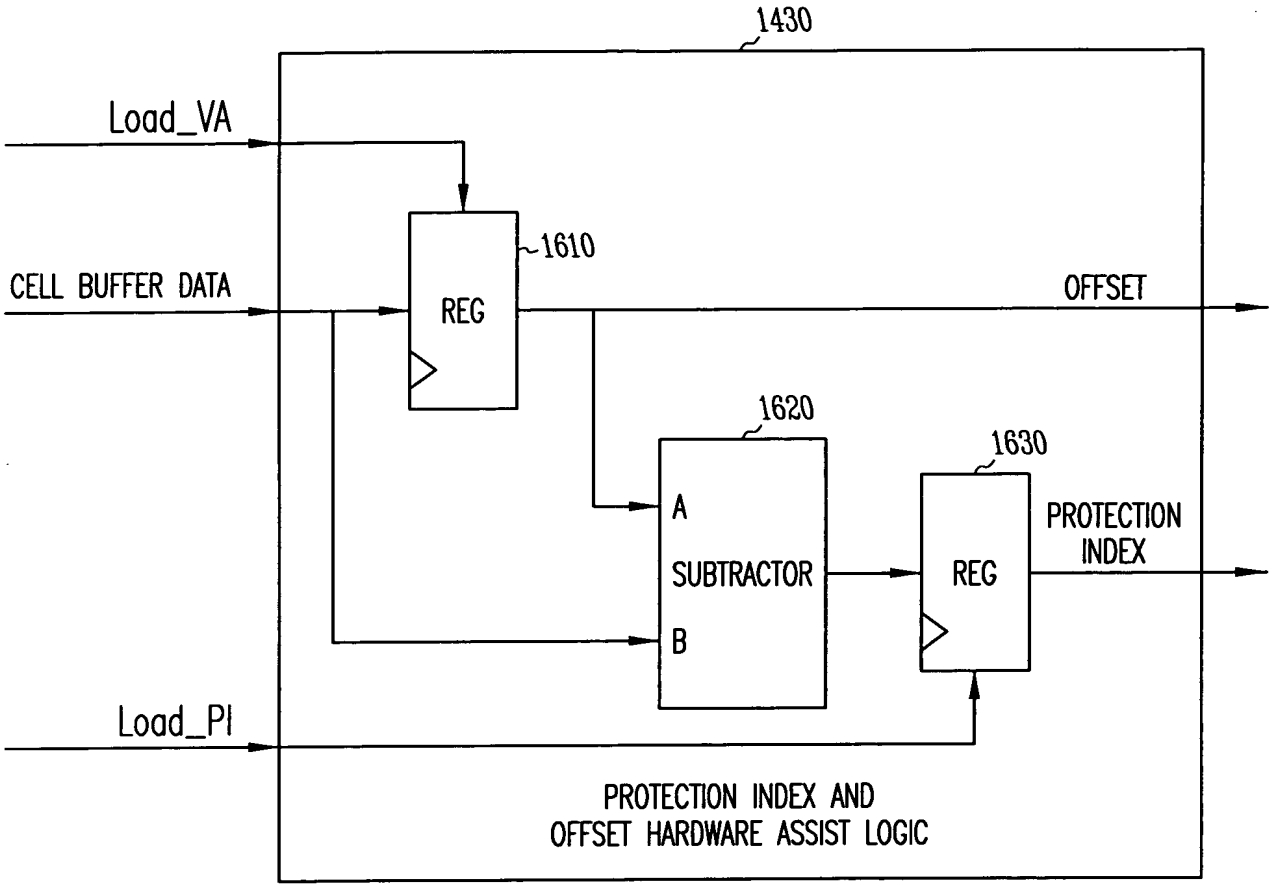

1430
Load_VA
CELL BUFFER DATA
REG
1610
OFFSET
1620
1630
A
SUBTRACTOR
B
REG
PROTECTION INDEX
Load_PI
PROTECTION INDEX AND
OFFSET HARDWARE ASSIST LOGIC

FIG. 16

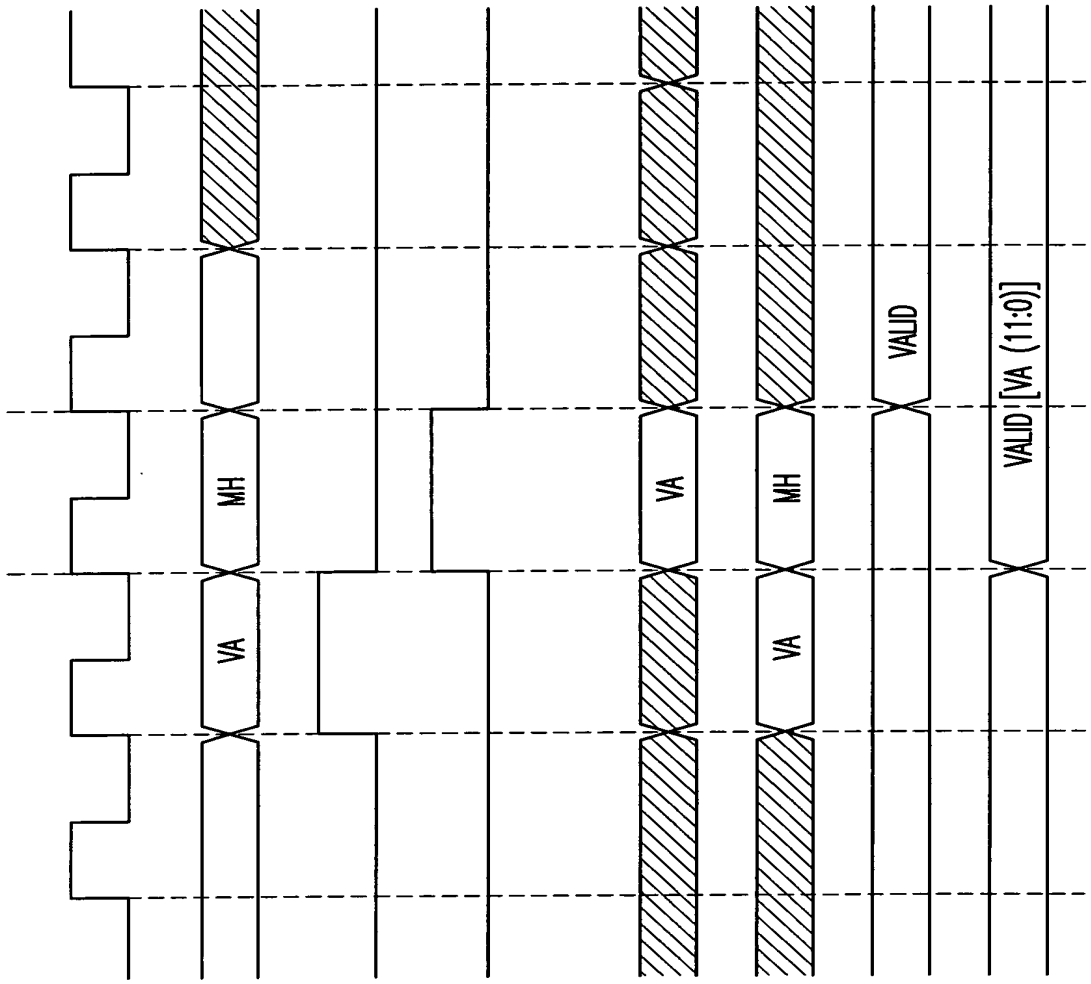


FIG. 17A

FIG. 17B

FIG. 17C

FIG. 17D

FIG. 17E

FIG. 17F

FIG. 17G

FIG. 17H